CLAIMS

We Claim:

1 A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:

(a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions; and

(b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

2 The method of claim 1 wherein step (b) further includes the step of: prioritizing the dummy regions such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.

3 The method of claim 2 further including the step of: allowing a user to specify a clock net criticality value for the clock nets.

4 The method of claim 3 wherein step (b) further includes the step of: in an absence of a user-specified clock net criticality value for any of the clock nets, assigning a default value.

5 The method of claim 4 wherein step (b) further includes the step of: prioritizing the dummy regions such that between two dummy regions located adjacent to clock net wires of the same width, the dummy region that is adjacent to a clock net having a higher criticality value is filled with dummy metal after the other dummy region.

6 The method of claim 5 wherein step (b) further includes the step of: calculating a timing factor for each dummy region located adjacent to a clock net by multiplying a width of the clock net wire by the clock net criticality value.

7 The method of claim 6 wherein step (b) further includes the step of: assigning a timing factor value of 0 to all dummy regions not adjacent to a clock-net wire.

8 The method of claim 7 further including the step of: maintaining a dummy region list for each tile in the design.

9 The method of claim 8 wherein step (b) further includes the step of: sorting the timing factors assigned to each of the dummy regions in the list in order to prioritize the dummy regions in the tile.

10 The method of claim 9 wherein step (b) further includes the step of: inserting dummy metal into the dummy regions starting with the first dummy region on the list until a minimum density requirement for the tile is met.

11 The method of claim 10 wherein step (b) further includes the step of: after each dummy metal insertion, adding the area of the inserted dummy metal to an interconnect area property of the tile.

12 The method of claim 11 wherein step (b) further includes the step of: calculating a dummy metal area that needs to be inserted in the tile to meet a minimum density requirement as:

Dummy Metal Area = (Minimum Density * Tile Area) - Interconnect Area

13 The method of claim 1 wherein step (a) further includes the step of: initializing a dummy region list for each tile as a single rectangle corresponding to the outline of the tile.

14 The method of claim 13 wherein step (a) further includes the step of: traversing a design database and for each object found in the current tile, subtracting an outline of the object from the dummy region on which it lies.

15 The method of claim 14 wherein step (a) further includes the step of: once an object is found intersecting a particular dummy region,

(i) adding an area of the object to an interconnect area property for the tile,

(ii) partitioning the dummy region into sub-dummy regions,

(iii) removing the dummy region from the dummy region list, and

(iv) adding the sub-dummy regions to the dummy region list.

16 The method of claim 15 wherein step (a) further includes the step of: if a particular object is a wire on a clock net, storing a width of the wire as a clock net width property of the dummy region created by an outline of the object, and tagging an edge of each dummy region located immediately adjacent to the clock net wire with a clock net edge property.

17 The method of claim 16 wherein step (b) further includes the step of: calculating a timing factor for each dummy region in the list that has a clock net width property, and sorting the dummy regions based on the timing factors.

18 A computer-readable medium containing program instructions for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the program instructions for:

(a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions; and

(b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

19 The computer-readable medium of claim 18 wherein instruction (b) further includes the instruction of: prioritizing the dummy regions such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.

20 The computer-readable medium of claim 19 further including the instruction of: allowing a user to specify a clock net criticality value for the clock nets.

21 The computer-readable medium of claim 20 wherein instruction (b) further includes the instruction of: in an absence of a user-specified clock net criticality value for any of the clock nets, assigning a default value.

22 The computer-readable medium of claim 21 wherein instruction (b) further includes the instruction of: prioritizing the dummy regions such that between two dummy regions located adjacent to clock net wires of the same width, the dummy region that is adjacent to a clock net having a higher criticality value is filled with dummy metal after the other dummy region.

23 The computer-readable medium of claim 22 wherein instruction (b) further includes the instruction of: calculating a timing factor for each dummy region located adjacent to a clock net by multiplying a width of the clock net wire by the clock net criticality value.

24 The computer-readable medium of claim 23 wherein instruction (b) further includes the instruction of: assigning a timing factor value of 0 to all dummy regions not adjacent to a clock-net wire.

25 The computer-readable medium of claim 24 further including the instruction of: maintaining a dummy region list for each tile in the design.

26 The computer-readable medium of claim 25 wherein instruction (b) further includes the instruction of: sorting the timing factors assigned to each of the dummy regions in the list in order to prioritize the dummy regions in the tile.

27 The computer-readable medium of claim 26 wherein instruction (b) further includes the instruction of: inserting dummy metal into the dummy regions starting with the first dummy region on the list until a minimum density requirement for the tile is met.

28 The computer-readable medium of claim 27 wherein instruction (b) further includes the instruction of: after each dummy metal insertion, adding an area of the inserted dummy metal to an interconnect area property of the tile.

29 The computer-readable medium of claim 28 wherein instruction (b) further includes the instruction of: calculating a dummy metal area that needs to be inserted in the tile to meet a minimum density requirement as:

Dummy Metal Area = (Minimum Density * Tile Area) - Interconnect Area

30 The computer-readable medium of claim 18 wherein instruction (a) further includes the instruction of: initializing a dummy region list for each tile as a single rectangle corresponding to the outline of the tile.

31 The computer-readable medium of claim 30 wherein instruction (a) further includes the instruction of: traversing a design database and for each object found in the current tile, subtracting an outline of the object from the dummy region on which it lies.

32 The computer-readable medium of claim 31 wherein instruction (a) further includes the instruction of: once an object is found intersecting a particular dummy region,

(i) adding an area of the object to an interconnect area property for the tile,

(ii) partitioning the dummy region into sub-dummy regions,

(iii) removing the dummy region from the dummy region list, and

(iv) adding the sub-dummy regions to the dummy region list.

33 The computer-readable medium of claim 32 wherein instruction (a) further includes the instruction of: if a particular object is a wire on a clock net, storing an width of the wire as a clock net width property of the dummy region created by an outline of the object, and tagging an edge of each dummy region located immediately adjacent to the clock net wire with a clock net edge property.

34 The computer-readable medium of claim 33 wherein instruction (b) further includes the instruction of: calculating a timing factor for each dummy region in the list that has a clock net width property, and sorting the dummy regions based on the timing factors.

35 A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:

(a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions;

(b) determining which of the dummy regions are located adjacent to clock nets;

(c) assigning a timing value to each dummy region based on an width of an adjacent clock net wire;

(d) sorting the dummy regions based on the timing factors; and

(e) inserting dummy metal into the sorted dummy regions such that the dummy regions located adjacent to increasingly wider clock nets are filled last, thereby minimizing any timing impact on the clock nets.

36 The method at claim 35 wherein step (c) further includes the steps of: assigning the timing factor based on the width of the clock net wire and a user-specified timing criticality value assigned to the clock net.

37 The method of claim 26 wherein step (e) further include the step of: inserting dummy metal into the sorted dummy regions one by one until a minimum density requirement for a current tile is met.